

ASYNCHRONOUS MULTIPLE-ORDER ISSUE SYSTEM ARCHITECTURE

ABSTRACT OF THE DISCLOSURE

An asynchronous circuit is described for processing units of data having a program order associated therewith. The circuit includes an N-way-issue resource comprising N parallel pipelines. Each pipeline is operable to transmit a subset of the units of data in a first-in-first-out manner. The asynchronous circuit is operable to sequentially control transmission of the units of data in the pipelines such that the program order is maintained.